CE-ATA Technical Errata

Errata ID	**Protocol 003**
Affected Spec Ver.	**Protocol 1.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
Amber Huffman	Intel	04/12/2005

Description of the specification technical flaw (add space as needed)

The Idle state in the device ATA state machine is missing a transition to stay within that state if the Command and Control registers are not written. This errata corrects the DA_Idle state by adding the transition that remains in the DA_Idle state if the first two transition conditions are not true.

Description of the correction

Modify state DA2: DA_Idle in section 2.4.3 as shown:

DA2: DA_Idle	Clear BSY=0, set DRDY=1, and clear DRQ=0 in the Status register.	
1. Command register written by MMC layer	→	DA_ ATADecode
2. Control register written by MMC layer and SRST[1] bit set to one	→	DA_SR_Cmd
3. Command register not written by MMC layer and (Control register not written by MMC layer with SRST bit set to one)	→	DA_Idle
NOTE: 1. This transition is taken regardless of the state the device is in. For the sake of clarity, this transition is not replicated on all the other device ATA states. The SRST bit shall only be set to 1 by the host using the FAST_IO (CMD39) command.		

Disposition log

04/12/2005	Erratum captured
06/17/2005	Erratum ratified